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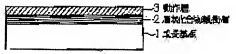
(54) MANUFACTURE OF WAFER FOR SEMICONDUCTOR ELEMENT AND SEMICONDUCTOR ELEMENT ITSELF

(57)Abstract:
PURPOSE: To manufacture the semiconductor element at high yield by a method wherein a buffer layer comprising lamellar compound having excellent cleavage strength is provided between a deposition substrate and an actuation layer so as to easily release the actuation layer only to be recovered without damaging the same at all.
CONSTITUTION: A buffer layer 2 comprising lamellar compound having excellent cleavage strength is provided on a depositing substrate 1. Next, an actuation layer 3 is formed. The title semiconductor element is formed of the actuation layer 3 using fine processing technology. At this time, due to the buffer layer 2 comprising inter-layers thereof coupled with one another by van der Waals' force, the depositing substrate 1 can be easily released from the actuation layers 3 by the cleavage strength. That is, the depositting substrate 1 can be released by sticking an adhesive tape to the actuation layer 3 or the depositing substrate itself. Furthermore, when the lamellar compound of the buffer layer 2 is left on the actuation layer 3, the residual lamellar compound can be perfectly removed by repeatedly releasing said compound using the same adhesive tape.



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(54)【発明の名称】　半導体素子用ウエハ及び半導体素子の製造方法

(57)【要約】

【目的】　動作層を破損することなく、成長基板から動作層のみを容易に除去することのできる半導体素子用ウエハ及び該ウエハを使用して半導体素子を高い歩留りで製造することのできる方法を提供しようとするものである。

【構成】　成長基板と動作層の間に劈開性の優れた層状化合物からなる緩衝層を備えたことを特徴とする半導体素子用ウエハ、及び、成長基板上に劈開性の優れた層状化合物からなる緩衝層を形成し、該緩衝層上に動作層をエピタキシャル成長した後、上記動作層と成長基板を剥離し、半導体素子用支持基板に接合することを特徴とする半導体素子の製造方法である。

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【特許請求の範囲】

【請求項1】　成長基板上にエピタキシャル動作層を有する半導体素子用ウエハにおいて、成長基板と動作層の間に劈開性の優れた層状化合物からなる緩衝層を備えたことを特徴とする半導体素子用ウエハ。

【請求項2】　エピタキシャル動作層を有する半導体素子の製造方法において、成長基板上に劈開性の優れた層状化合物からなる緩衝層を形成し、該緩衝層上に動作層をエピタキシャル成長した後、上記動作層と成長基板を剥離し、半導体素子用支持基板に接合することを特徴とする半導体素子の製造方法。

【請求項3】　エピタキシャル動作層を有する半導体素子の製造方法において、成長基板上に劈開性の優れた層状化合物からなる緩衝層を形成し、素子形成領域以外の該緩衝層の一部を少なくとも除去して成長基板を露出させ、該成長基板の露出部分及び該緩衝層上に動作層をエピタキシャル成長させた後、素子形成領域のみを切断して取り出し、素子領域の動作層を成長基板から剥離し、半導体素子用支持基板に接合することを特徴とする半導体素子の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、化合物半導体の成長基板を有しない高出力半導体素子、赤外撮像素子などに適した半導体素子用ウエハ及び半導体素子の製造方法に関する。

【0002】

【従来の技術】従来、半導体素子に用いられるエピタキシャルウエハは、例えばサイエンスフォーラム「最新化合物半導体ハンドブック」（昭和57年7月10日発行）第313～323頁に示されているように、基板上に成長基板と同一結晶構造の緩衝層と動作層を積層した構造からなっている。この素子は、素子の熱抵抗を低減するためには、成長基板及び緩衝層を可能な限り薄くするか、完全に除去する必要がある。また、赤外撮像素子においては、上記ハンドブック第349～350頁に示されているように、光の吸収層となる基板を完全に除去する必要がある。

【0003】

【発明が解決しようとする課題】従来、この種のエピタキシャルウエハは、動作層、緩衝層及び成長基板が同一の結晶構造で構成されている。図5は、従来のエピタキシャルウエハの断面図であり、化合物半導体成長基板8の上にエピタキシャル成長させた緩衝層9及びさらにエピタキシャル成長させた動作層10からなるウエハである。かかるウエハから動作層を得るためには、従来、研磨、あるいはエッチングによって、成長基板、あるいは、緩衝層及び成長基板を動作層から除去していたが、動作層を破損せずに、同一の結晶構造の成長基板、あるいは、緩衝層及び成長基板を均一に除去することは極めて困難であった。そこで、本発明は、上記の欠点を解消し、動作層を破損することなく、成長基板を除去することができる半導体素子用ウエハ及び該ウエハを使用する半導体素子の製造方法を提供しようとするものである。

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【0004】

【課題を解決するための手段】本発明は、（1）基板上にエピタキシャル動作層を有する半導体素子用ウエハにおいて、基板と動作層の間に劈開性の優れた層状化合物からなる緩衝層を備えたことを特徴とする半導体素子用ウエハ、（2）エピタキシャル動作層を有する半導体素子の製造方法において、基板上に劈開性の優れた層状化合物からなる緩衝層を形成し、該緩衝層上に動作層をエピタキシャル成長した後、上記動作層と基板を剥離し、新たな基板に接合することを特徴とする半導体素子の製造方法、及び、（3）エピタキシャル動作層を有する半導体素子の製造方法において、成長基板上に劈開性の優れた層状化合物からなる緩衝層を形成し、素子形成領域以外の該緩衝層の一部を少なくとも除去して成長基板を露出させ、該成長基板の露出部分及び該緩衝層上に動作層をエピタキシャル成長させた後、素子形成領域のみを切断して取り出し、素子領域の動作層を成長基板から剥離し、半導体素子用支持基板に接合することを特徴とする半導体素子の製造方法である。なお、緩衝層として用いる上記の劈開性の優れた層状化合物は、層間をファンーデアーワールス力（分子性結合力）で結合するものであることが好ましく、具体的にはMoS$_2$、NbS$_2$、MoSe$_2$、NbSe$_2$、GaSe、SnS$_2$、SnSe$_2$、InSeなどを挙げることができる。また、成長基板としては、動作層と同一の結晶構造を有する単結晶基板を使用することが好ましく、基板の結晶方位は（111）面が好ましい。

【0005】

【作用】図1は、本発明の1具体例である半導体素子用ウエハの断面図であり、成長基板1の上に劈開性の優れた層状化合物からなる緩衝層2を設け、次いで、動作層3を形成したものである。半導体素子は、動作層3に微細加工技術で素子を形成する。そして、緩衝層2は、層間がファンーデアーワールス力で結合されているため、劈開により動作層3から成長基板1を容易に剥がすことができる。この剥離は、動作層3、あるいは、成長基板1に粘着テープを張りつけて機械的に容易に剥がすことができる。また、動作層3に緩衝層2の層状化合物が残る場合は、粘着テープを用いて再度剥離操作を行うことにより、完全に除去することが可能である。このようにして得た動作層3は、ヒートシンクあるいはガラス基板等の半導体素子用支持基板に接合することにより、所望の半導体素子を形成することができる。ヒートシンクは、素子から発生する熱を外部に効率的に放散するためのものであり、熱伝導率の大きな材質が用いられる。絶縁体ではダイヤモンド、ベリリア、アルミナなど、ま

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た、半導体ではシリコンなど、導電体では金、銀、銅などが使用される。このような半導体素子は、成長基板を全く含まないため、熱抵抗を低減することができ、光吸収層の除去のための研磨やエンチングを行う必要がなく、動作層の破損を回避することが可能になった。

【０００６】図２は、本発明の他の具体例である半導体素子用ウエハの平面図であり、図３は、図２のＡ－Ａ断面図である。成長基板１の上に劈開性の優れた層状化合物からなる緩衝層２を設け、素子形成領域４以外の緩衝層２を微細加工により適当な間隔でエッチングして除去し、緩衝層除去領域５を形成し、次いで、緩衝層除去領域５の成長基板の上及び緩衝層２の上に動作層３を形成する。そして、ダイシング部６に沿って切断して成長基板１、層状化合物緩衝層２及び動作層３からなる素子形成領域４のチップを得る。ここで、緩衝層２は、層状化合物の層間がファン－デア－ワールス力で結合されているため、劈開により動作層３から成長基板１を容易に剥がすことができる。即ち、図１と同様に、動作層３を剥離し、図４のように、半導体素子用支持基板７に接合して半導体素子を形成する。

【０００７】

【実施例】ＧａＡｓ（１１１）Ｂ面基板上に、ＭＢＥ法で厚さ１００ÅのＧａＳｅ緩衝層を成長させ、次いで、同法で厚さ０．１μmのｐ－ＡｌＧａＡｓ窓層、１０μmのｐ－ＧａＡｓ光吸収層、厚さ０．３μmのｎ－ＡｌＧａＡｓ活性層からなる動作層を成長させた。さらに、

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表面にオーミック電極とショットキー電極を形成してＣＣＤイメージセンサーの基本素子を作製した。素子を形成したウエハの表面に樹脂で保護板を張り付け、基板には粘着テープを張り付けて機械的に剥離した。動作層の裏面に緩衝層が残っていたので、再度緩衝層に粘着テープを張り付けて剥離したところ、緩衝層のＧａＳｅを完全に除くことができた。得られた動作層をガラス基板に接合してＣＣＤイメージセンサーの基本素子を形成した。この素子の特性を調べたところ、暗電流は従来の基板をエッチングによって完全に除去して作製した素子と同程度以上であり、遜色がなかった。

【０００８】

【発明の効果】本発明は、上記の構成を採用することにより、動作層を破損することなく、動作層のみを容易に剥離回収することができ、高品位の半導体素子を高い歩留りで製造することが可能になった。

【図面の簡単な説明】

【図１】本発明の１具体例である半導体素子用ウエハの断面図である。

【図２】本発明の他の具体例である半導体素子用ウエハの平面図である。

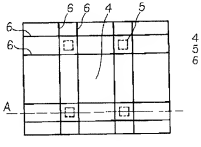
【図３】図２のＡ－Ａ断面図である。

【図４】動作層を半導体素子用支持基板に接合したウエハの断面図である。

【図５】従来の半導体素子用ウエハの断面図である。

【図１】

【図２】



【図３】

【図４】

【図５】

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(54) [Title of the Invention] WAFER FOR SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

(57) Abstract

[Object] To provide a wafer for a semiconductor device, in which only an operation layer can be easily removed from a grown substrate without damaging the operation layer, and a method capable of manufacturing the semiconductor device with a high yield by use of the wafer.

[Constitution] Provided is a wafer for a semiconductor device characterized in that a buffer layer formed of a layered compound having an excellent cleavage is provided between a grown substrate and an operation layer. Furthermore, provided is a method of manufacturing the semiconductor device, in which after the buffer layer formed of the layered-like compound having the excellent cleavage is formed on the grown substrate, the operation layer is epitaxially grown on the buffer layer, and the operation layer and the grown substrate are peeled off from each other, thus the operation layer is joined to a supporting substrate for the semiconductor device.

[Scope of claims]

[Claim 1] A wafer for a semiconductor device having an epitaxial operation layer on a grown substrate, the wafer for a semiconductor device being characterized in that a buffer layer formed of a layered compound having an excellent cleavage is provided between a grown substrate and an operation layer.

[Claim 2] A method of manufacturing a semiconductor device having an epitaxial operation layer, the method being characterized in that after a buffer layer formed of a layered-like compound having an excellent cleavage is formed on a grown substrate, an operation layer is epitaxially grown on the buffer layer, and the operation layer and the grown substrate are peeled off from each other, thus the operation layer is joined to a supporting substrate for the semiconductor device.

[Claim 3] A method of manufacturing a semiconductor device having an epitaxial operation layer, the method being characterized in that a buffer layer formed of a layered

compound having an excellent cleavage is formed on a grown substrate; the grown substrate is exposed by removing at least a part of the buffer layer except for a device formation region; an operation layer is epitaxially grown on an exposed portion of the grown substrate and the buffer layer; only the device formation region is cut to be taken out; and the operation layer in the device region is peeled off from the grown substrate to be jointed to a supporting substrate for the semiconductor device.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Applicability] The present invention relates to a wafer for a semiconductor device suitable for a high output semiconductor device, an infrared image pick-up device, which has no growth substrate of a compound semiconductor, and a method of manufacturing a semiconductor device.

[0002]

[Prior Art] Conventionally, an epitaxial wafer used for a semiconductor device has a structure in which an operation layer and a buffer layer having the same crystal structure as that of a grown substrate are laminated on a substrate, as shown, for example, in Science Forum "Latest Compound Semiconductor Handbook", pages 313 to 323, issued on July 10, 1982. In this device, in order to reduce a heat resistance of the device, the grown substrate and the buffer layer need to be made as thin as possible, or they need to be removed thoroughly. Furthermore, in an infrared image pick-up device, a substrate serving as an absorption layer of light needs to be removed thoroughly, as shown in the foregoing Handbook, pages 349 to 350.

[0003]

[Problem to be Solved by the Invention] Conventionally, an epitaxial wafer of such a kind is composed of an operation layer, a buffer layer and a grown substrate, which have the same crystal structure. Fig. 5 is a sectional view of the conventional epitaxial wafer, which is a wafer composed of a buffer layer 9 epitaxially grown on a compound semiconductor grown substrate 8, and an operation layer 10 epitaxially grown thereon. In order to obtain such operation layer from the wafer, the grown substrate, or the buffer layer and the grown substrate, was removed from the operation layer by polishing or etching. It was very difficult to uniformly remove the grown substrate, or the buffer layer and the grown substrate, which have the same crystal structure, without breaking the operation layer. Accordingly, the present invention is to provide a wafer for a semiconductor device with which the foregoing drawbacks are solved, and in which the grown substrate is removed without breaking the operation layer, and to provide a method of manufacturing a semiconductor device using the wafer.

[0004]

[Means for Solving the Subjects] (1) The present invention is a wafer for a semiconductor device having an epitaxial operation layer on a substrate, the wafer for a semiconductor device being characterized in that a buffer layer formed of a layered compound having an excellent cleavage is provided between the substrate and the operation layer. (2) The present invention is a method of manufacturing a semiconductor device having an epitaxial operation layer, the method being

characterized in that after a buffer layer formed of a layered compound having an excellent cleavage is formed on a substrate, an operation layer is epitaxially grown on the buffer layer, and the operation layer and the substrate are peeled off from each other, thus it is joined to a new substrate. (3) The present invention is a method of manufacturing a semiconductor device having an epitaxial operation layer, the method being characterized in that a buffer layer formed of a layered compound having an excellent cleavage is formed on a grown substrate; the grown substrate is exposed by removing at least a portion of the buffer layer except for a device formation region; an operation layer is epitaxially grown on an exposed portion of the grown substrate and the buffer layer; only the device formation region is cut to be taken out; and the operation layer in the device region is peeled off from the grown substrate to be joined to a supporting substrate for the semiconductor device. The foregoing compound having the excellent cleavage used as the buffer layer should be the one in which layers are bonded with Van der Waals force (molecular bonding force). To be more specific, MoS_2, NbS_2, $MoSe_2$, $NbSe_2$, GaSe, SnS_2, $SnSe_2$ and $InSe_2$ are enumerated as the layered compound. Furthermore, as the grown substrate, a single crystal substrate having the same crystal structure as that of the operation layer should be used, and a crystal orientation of the substrate should be a (111) plane.

[0005]

[Operation] Fig. 1 is a sectional view of a wafer for a semiconductor device which is a concrete example of the present invention. A buffer layer 2 formed of a layered-like compound having an excellent cleavage is provided on a grown substrate 1. Subsequently, the operation layer 3 is formed. As to the semiconductor device, the device is formed in the operation layer 3 by use of a micro processing technology. Then, since the layers are bonded with the Van der Waals force in the buffer layer 2, it is possible to peel off the grown substrate 1 from the operation layer 3 by cleavage easily. In this peeling-off, an adhesion tape is adhered to the operation layer 3 or the grown substrate 1, and the grown substrate 1 can be easily peeled off from the operation layer 3 mechanically. Furthermore, when the layered compound of the operation layer 3 remains in the operation layer 3, the peeling-off operation is performed by use of the adhesive tape again, whereby it is possible to remove the grown substrate 1 thoroughly. The operation layer 3 obtained in the above-described manner is bonded to a supporting substrate for the semiconductor device such as a heat sink and a glass substrate, whereby the desired semiconductor device can be formed. The heat sink is for effectively discharging heat generated by the device to the outside, and a material having a high thermal conductivity is used as the heat sink. Diamond, beryllia, alumina or the like is used when the heat sink is an insulating material. Silicon or the like is used when the heat sink is a semiconductor. Gold, silver, copper or the like is used when the heat sink is a conductive material. Since such semiconductor device does not include a grown substrate at all, it is possible to reduce a heat resistance, and polishing and etching for removing a light absorption layer need not to be performed, and thus it was made possible to avoid the break-down of an operation layer.

[0006] Fig. 2 is a plan view of a wafer for a semiconductor

device, which is another concrete example of the present invention. Fig. 3 is a sectional view taken along the line A-A of Fig. 2. A buffer layer 2 formed of a layered compound having an excellent cleavage is provided on a grown substrate 1, and portions of the buffer layer 2 except for a device formation region 4 are removed by etching them at suitable intervals with micro processing. Thus, a buffer layer removing region 5 is formed, and subsequently an operation layer 3 is formed on the grown substrate and the buffer layer 2 corresponding to the buffer layer removing region 5. Then, a chip of the device formation region 4 composed of the grown substrate 1, the layered compound buffer layer 2 and the operation layer 3 is obtained by cutting them along a dicing portion 6. Herein, since the layers of the layered compound are bonded by a Van der Waals force, it is possible to peel off the grown substrate 1 from the operation layer 3 easily by cleavage. Specifically, in the same manner as in the case of Fig. 1, the operation layer 3 is peeled off, and the semiconductor device is formed by bonding the operation layer 3 to a supporting substrate 7 for the semiconductor device.

[0007]

[Example] A GaSe buffer layer having a thickness of 100Å was grown on a GaAs (111) B plane substrate by an MBE method, and subsequently an operation layer composed of a p-AlGaAs window layer having a thickness of 0.1 μm, a p-GaAs light absorption layer having a thickness of 10μm and an n-AlGaAs active layer having a thickness of 0.3μm was grown by the MBE method. Furthermore, an ohmic electrode and a Schottky electrode were formed on the surface thereof, thus fabricating a basic device of a CCD image sensor. By use of resin, a protection plate was adhered to the surface of the wafer where the device was formed, and an adhesion tape was adhered to the substrate to be mechanically peeled off. Since the buffer layer remained on the back surface of the operation layer, an adhesion tape was adhered thereto again to be peeled off. Thus, GaSe of the buffer layer could be removed thoroughly. The operation layer obtained was joined to a glass substrate, and a basic device of a CCD image sensor was formed. When the characteristics of this device was examined, a dark current thereof was substantially not less than that of a conventional device fabricated by removing a substrate thoroughly by etching. The obtained device stood comparison therewith.

[0008]

[Effects of the Invention] The present invention adopts the foregoing constitution, whereby it is possible to peel off and recover only the operation layer without damaging the operation layer. Accordingly, it is possible to manufacture high quality semiconductor devices with a high yield.

[Brief Description of the Drawings]

[Figure 1] Fig. 1 is a sectional view of a wafer of a semiconductor device which is one concrete example of the present invention.

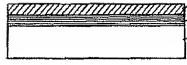
[Figure 2] Fig. 2 is a plan view of a wafer for a semiconductor device which is another concrete example of the present invention.

[Figure 3] Fig. 3 is a sectional view taken along the line A-A of Fig. 2.

[Figure 4] Fig. 4 is a sectional view of the wafer in which an operation layer is bonded to a supporting substrate for the semiconductor device.

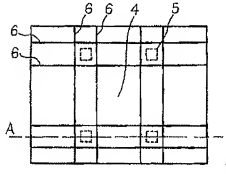
[Figure 5] Fig. 5 is a sectional view of a conventional wafer for a semiconductor device.

Fig.1



OPERATION FILM
LAYERED COMPOUND BUFFER LAYER
GROWN SUBSTRATE

Fig.2

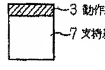


4：素子形成部 DEVICE FORMATION REGION
5：緩衝層除去部 BUFFER LAYER REMOVING REGION
6：ダイシング部 DICING PORTION

Fig.3

OPERATION FILM
LAYERED COMPOUND BUFFER LAYER
GROWN SUBSTRATE

Fig.4



OPERATION LAYER
SUPPORTING SUBSTRATE

Fig.5

OPERATION LAYER
BUFFER LAYER
GROWN SUBSTRATE

1 GROWN SUBSTRATE
2 LAYERED COMPOUND BUFFER LAYER
3 OPERATION FILM

FIG. 1
1 GROWN SUBSTRATE
2 LAYERED COMPOUND BUFFER LAYER
3 OPERATION FILM

FIG. 2
4 DEVICE FORMATION REGION
5 BUFFER LAYER REMOVING REGION
6 DICING PORTION

FIG. 3
1 GROWN SUBSTRATE
2 LAYERED COMPOUND BUFFER LAYER
3 OPERATION FILM

FIG. 4
3 OPERATION LAYER
4 SUPPORTING SUBSTRATE

FIG. 5
8 GROWN SUBSTRATE
9 BUFFER LAYER
10 OPERATION LAYER